

Platform Processor Verification at P.A. Semi



P.A. Semi's Verification Challenge



P.A. Semi is a fabless semiconductor startup developing the ultra-low power, high performance PWRficient processor family for high-performance embedded and computing applications such as datacom and telecom, storage, entry-level servers and game consoles. Its first chip is an SoC consisting of two general purpose CPU's, caches and IO interfaces. With a complexity of more than 20M logic gates to verify across a large suite of tests, OSes, and applications, the P.A. Semi engineering team knew that a design this sophisticated would necessitate the most advanced verification tools available, most notably hardware-assisted verification.

The P.A. Semi team is comprised of industry veterans with emulation experience from a multitude of past projects. From the start, the team was determined to find a solution that would offer speedy verification without the laborious mapping process. They conducted an evaluation of the latest emulation products on the market to determine how each would perform. P.A. Semi's benchmark showed that EVE's ZeBu system had excellent performance at a reasonable price and satisfied its requirements on both internal clock and transactor interface speed. In addition, ZeBu was easier to set up. Consequently, P.A. Semi purchased one ZeBu-ZV and two ZeBu-XL systems as its hardware verification platforms.

Verification Flow

The P.A. Semi team begins the verification process with simulation at the RTL level using C++ testbenches and transactors linking to NC-sim via the PLI. One example of the transactors is a DRAM

transactor built with a sparse memory model. A series of diagnostic routines is used to exercise the processors, on-chip bus, L2 cache and memory interface, in directed and random fashion. The simulation model executes the tests at an average rate of 200 clocks/sec on a farm of workstations. Random tests are run continuously while the engineers debug and fix the failures. When the failure rate declines to less than one every few thousand tests, they shift to high-speed emulation with ZeBu running at about five thousand times faster than simulation. This reduces the simulation throughput bottleneck tremendously, allowing the engineers to quickly find rare corner cases that could take months of simulation times.

Verification Environment

The ZeBu verification environment is set up to mirror exactly that of the simulation. The same testbenches, transactors and test programs are used in both environments. The primary differences are two: the RTL model of the design is mapped into ZeBu, and the PLI interface between the RTL model and testbenches and transactors is replaced with EVE's SCEMI interface. The effective speed of this environment is one million clocks/sec, or 5000x faster than simulation, enabling the P.A. Semi engineers to run hundreds of thousands tests every day.

Using this setup, the P.A. Semi team employed a hierarchical approach, verifying major blocks such as floating point unit first, then working their way up to full CPU and full chip models. The tests they run start from short diagnostics, followed by booting VxWorks and Linux and running application programs. Booting OSes and running applications prove to be invaluable since it helps uncover bugs that are not exposed even after millions of random test cases have been simulated.



ZeBu Case Study

What P.A. Semi Likes Most About ZeBu

“With ZeBu’s huge throughput we were able to rely on random testing, high level diagnostics, and OS booting instead of manually-written tests. That option saved us significant engineering resources. The system has paid for itself in manpower savings alone.”

“ZeBu’s SCEMI interface is amazingly fast for linking our C++ transactors to the emulator. EVE gives us access to all the APIs, making it easy for us to create an efficient verification environment. We were able to leverage the testbenches and transactors that we used in simulation, but run them 5000 times faster!”

Mike Dickman, Sr. Principal Verification Engineer

The Bottom Line

The P.A. Semi team of veterans demanded the most sophisticated verification equipment available to assist in the development of its advanced PWRficient processors. After conducting in-house tests, the team identified the ZeBu-ZV and ZeBu-XL as the best hardware verification tools to ensure that even the most obscure bugs are found prior to tapeout.