

IP Verification at Seagate Technology

Seagate's Verification Challenge



Seagate is the worldwide leader in the design, manufacturing and marketing of hard disc drives, providing products for a wide range of Enterprise, Desktop, Mobile Computing, and Consumer Electronics applications.

Seagate's advanced architecture group is responsible for developing IP blocks that will be incorporated in the company's next generation disc controller ASICs. Some of these IP blocks will be used in several different products, and it is imperative that the designs be exhaustively verified under all possible operating conditions prior to release.

Seagate had previously relied on simulation as their primary verification tool for IP blocks, using a combination of ModelSim and Vera. Vera was used for constrained pseudo-random test bench generation, as a means to construct thousands of different combinations of commands and data packets. However, early in the design of a new compute-intensive IP block Seagate's architects calculated that it would take in the order of 500 CPU-years to simulate all the test cases necessary to prove out this particular design. With a six month design schedule it was clear that simulation alone would not be adequate. That's when Seagate turned to EVE's ZeBu-ZV for help.

Seagate's IP design presented some unique verification challenges. The block has a 32 bit interface, over which commands and data are loaded into the block using a packet-based protocol. Once the device is set up it then processes the data for about 4 seconds of real time, after which it presents the results over the same 32 bit interface. At an operating speed of 150MHz, 4 seconds represents 600,000,000 cycles. Seagate needed to run several hundred thousand of these test cases to fully verify the design.

Seagate's Verification Strategy

On this project Seagate used the ModelSim/Vera combination for their initial verification runs to prove basic functionality, using about 50 tests per command. Once the design was generally functional they switched to the combination of ZeBu and Vera to be able to run thousands of tests for each command.

To maximize performance, Seagate used synthesizable *transactors* as the interface between their Vera code on the PC and their emulated IP block in ZeBu. The transactors perform the conversion from high-level commands and data packets to bit-level signals using the ZeBu hardware. The SCE-MI standard from Accellera defines how such transactors are written: they consists of an API on the software side to exchange high-level packets or messages, and a synthesizable BFM or state machine that gets mapped into the hardware platform.

To accelerate the simulation even further, Seagate took advantage of a property of this particular IP block: the only interaction between the Vera testbench and the IP block occurs during the initial setup of the test and the downloading of the results at the end of the run. In between these two interactions the design executes a huge number of cycles with no external communication whatsoever. Seagate exploited this fact by making ZeBu run in lock-step mode with Vera only during these interactions, and switching to a 15MHz clock supplied by ZeBu in between these accesses. To implement this solution, they simply changed the main clock of the design to switch between two inputs: the clock coming from Vera, and a clock generated by the ZeBu on-board clock generator.

Using this hybrid approach, Vera generated each new command and data combination, and then transferred the packet through a C function-call to the ZeBu transactors. Vera then switched ZeBu to the fast clock and initiated the test. ZeBu was able to run the tests at 15 MHz, equivalent to 1/10 of real time. Hence, in 40 seconds the test would



finish and ZeBu would signal Vera that it was ready to present the result. Meanwhile, Vera was computing the expected results in software, using the same algorithms implemented in the IP block. Once EVE and Vera completed their respective runs they would compare their results and flag any differences that occurred as errors.

Results of Using ZeBu

Seagate engineers were surprised that with their very first exposure to the system it took them only two hours to get their IP block compiled into ZeBu and running correctly. With a few more weeks of effort Seagate had implemented and debugged the transactor interface and had the system running at 15MHz.

In the first few days running on ZeBu Seagate engineers identified 25-30 new bugs in the design, which had escaped detection during simulation. In the five weeks to follow, Seagate ran ZeBu 24x7, generating hundreds of thousands of additional test cases. Through these runs Seagate identified 4 additional bugs that were very obscure corner cases related to specific sequences of commands. All of these bugs would likely have surfaced during product testing, but would have necessitated ASIC respins at a cost of \$500,000 or more.

Seagate plans to continue running additional test cases on ZeBu 24x7 until the resource is needed for another project. It takes only 1 hour/week to kick off new jobs and check the results of the previous runs, so there is little reason not to run the additional tests for added confidence.

What Seagate Likes Most About ZeBu:

- “In 6 hours we can now complete a year’s worth of simulation on ZeBu. That’s a 1400x speedup!”
- “The very first time we accessed the system we were able to compile our design into ZeBu and get our test cases running in less than 2 hours. EVE has done a great job automating the entire emulation flow.”
- “By using transactors we were able to integrate ZeBu directly with our Vera testbench with no simulator required. Not only did this eliminate the need for an additional simulation seat, it also freed up all the workstation resources for Vera computation, and hence maximized the performance of the overall system.”
- “Because ZeBu can be programmed via its PCI interface and accessed remotely, we are able to share a single ZeBu system among multiple design teams without requiring any physical access to the system. We manage it as a networked resource using an LSF queue, and ensure that the most important projects get highest priority access.”

The Bottom Line

“We would not be able to say that our IP was fully tested without the kind of exhaustive verification we performed using ZeBu. ZeBu helps us avoid ASIC respins for about a tenth of the cost of a single mask set.”

Don Matthews, Sr. Staff Design Engineer, Seagate